TMC2072

Genlocking Video Digitizer

Features

- · Fully integrated acquisition
- 3-channel video input multiplexer
- Two-stage (analog and digital) video clamp
- Automatic gain adjustment
- · Sync detection and separation
- · Pixel and subpixel adjustment of Hsync-to-video timing
- Genlock to any NTSC or PAL input, including PAL-M and PAL-N
- · Pixel clock generation
- 8-bit video A/D conversion
- Standard I²C-compatible R-bus microprocessor interface
- Fully-programmable line-locked pixel rates include:
 - 12.27 NTSC & PAL-M
 - 13.5 NTSC & all PAL
 - 14.75 PAL (non-M)
 - 15. PAL (non-M)
- Direct interface to Raytheon video encoders and decoders
- Built-in circuitry for crystal oscillator
- · No tuning or external voltage reference required
- Space-saving 100-lead MQFP package

Applications

- · Frame grabber
- Digital videotape recorders
- Desktop video

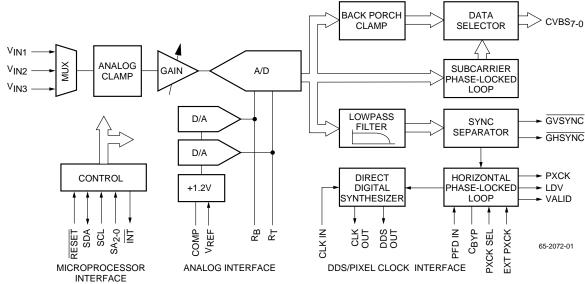
Description

The TMC2072 Genlocking Video Digitizer samples and quantizes standard analog baseband composite NTSC or PAL video into its 8-bit digital equivalent. It extracts horizontal and vertical sync signals, from which an on-chip PLL generates a line-locked pixel clock for the on-chip 8-bit A/D converter and a double-speed register clock to transfer data to a subsequent video processing subsystem. A second PLL generates a chroma subcarrier locked to the incoming chroma burst. The chip reports each line's color burst phase and frequency during the next horizontal sync pulse.

The TMC2072 includes a three-channel video input multiplexer, analog clamp, variable gain amplifier, and digital back porch clamp. The user may provide either an external 20MHz clock or a 20MHz crystal. No external component changes or tuning are required for PAL or NTSC operation at either D1 or square pixel VGA pixel rates.

The TMC2072 is fabricated in a submicron CMOS process and is packaged in a 100-lead MQFP. Its performance is guaranteed from 0 to 70° C.

Block Diagram



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